I CLAIM:

1. An apparatus for reducing noise effects associated with the vertical position of an on screen display (OSD) image for a display device that uses a vertical flyback signal and a horizontal flyback signal in producing an image, comprising:

a clock signal generator that is configured to produce multiple horizontal clock signals in response to the horizontal flyback signal, wherein each multiple horizontal clock signal has a different phase with respect to one another;

a phase selection circuit that is configured to select one of the multiple horizontal clock signals such that an edge associated with the selected multiple horizontal clock signal is non-coincident with an edge associated with the vertical flyback signal; and

a blanking circuit that is configured produce a blanking signal in response to the selected multiple horizontal clock signal such that the blanking signal determines the vertical position of the OSD image, whereby noise effects associated with at least one of the vertical flyback signal and the horizontal flyback signal are minimized.

2. The apparatus of Claim 1, wherein the horizontal clock signal generator produces the multiple horizontal clock signals in response to a horizontal rate signal and a scaled horizontal rate signal that is produced by a phase-locked loop circuit, wherein the scaled horizontal rate signal has a frequency that is a multiple of another frequency that corresponds to the horizontal rate signal.

3. The apparatus of Claim 2, wherein the phase-locked loop circuit produces at least one of the horizontal rate signal and the scaled horizontal rate signal in response to the horizontal flyback signal.

4. The apparatus of Claim 2, wherein the scaled horizontal rate signal has a scaled frequency that is double another frequency that corresponds to the horizontal rate signal.

5. The apparatus of Claim 2, wherein the horizontal rate signal and the scaled horizontal rate signal are dependent upon a predetermined resolution of the display device.

6. The apparatus of Claim 1, further comprising an interlace correction circuit that is arranged to selectively shift the phase of the multiple horizontal clock signals between each vertical frame period to compensate for a one-half line shift in the edge of the vertical flyback signal that occurs when the display device is in an interlace mode.

7. The apparatus of Claim 6, wherein the interlace correction circuit produces an interlace phase shift signal that is utilized by the clock signal generator to change the phase of each of the multiple horizontal clock signals.

8. The apparatus of Claim 1, wherein the selected horizontal clock signal has an associated clock period, and the selected horizontal clock signal is selected such that the edge associated with the selected horizontal clock signal occurs at least one-quarter of the clock period apart from the vertical flyback signal.

9. The apparatus of Claim 1, the phase selection circuit further comprising a combinational logic circuit that is configured to produce logic outputs that determine the selection of one of the multiple horizontal clock signals.

10. The apparatus of Claim 9, wherein the combinational logic circuit produces the logic outputs dependent upon a previous selection of one of the multiple horizontal clock signals.

11. The apparatus of Claim 1, wherein each adjacent multiple horizontal clock signal is substantially separated by 90 degrees.

12. The apparatus of Claim 1, wherein the vertical position of the OSD image is positioned within a display screen of the display device corresponding to a predetermined number of horizontal lines from a starting position on the display screen in response to the blanking signal.

13. A method for minimizing jitter in the vertical position of an on screen display (OSD) image associated with a display device having a display screen, comprising:

producing multiple horizontal clock signals that each have a different phase in response to a first horizontal timing signal and a second horizontal timing signal, wherein the first horizontal timing signal and the second horizontal timing signal are related;

selecting one of the multiple horizontal clock signals such that the occurrence of an edge associated with the selected horizontal clock signal is non-coincident with an edge associated with a vertical flyback signal of the display device; and

producing a vertical blanking signal in response to the selected horizontal clock signal wherein the vertical blanking signal triggers the display device to count a predetermined number of blank horizontal lines from the top of the display screen prior to generating the OSD image such that the predetermined number of blank horizontal lines corresponds to the vertical position of the OSD image on the display screen.

14. The method of Claim 13, further comprising generating one of the first horizontal timing signal and the second horizontal timing signal by a phase-locked loop circuit in response to a horizontal flyback signal of the display device.

15. The method of Claim 13, further comprising correcting the phase of each of the multiple horizontal clock signals for when the display device is operating in an interlace mode.

16. The method of Claim 15, further comprising shifting the phase of each of the multiple horizontal clock signals by 180 degrees between each vertical frame period to compensate for a one-half line delay in the edge of the vertical flyback signal that occurs between each vertical frame period when the display device is operating in the interlace mode.

17. The method of Claim 13, wherein selecting one of the multiple horizontal clock signals further comprises selecting one of the multiple horizontal clock signals depending on the multiple horizontal clock signal selected for a previous occurrence of the vertical flyback signal.

18. The method of Claim 13, wherein producing multiple horizontal clock signals further comprises producing each multiple horizontal clock signal such that each multiple horizontal clock signal has a phase that is 90 degrees apart from each adjacent multiple horizontal clock signal.

19. An apparatus for providing jitter reduction for an on screen display (OSD) window of a display device having a display screen, comprising:

a means for generating horizontal timing signals that is configured to generate a first horizontal timing signal and a second horizontal timing signal, wherein the first horizontal timing signal and the second horizontal timing signal are related;

a means for producing multiple horizontal clock signals that is configured to produce multiple horizontal clock signals in response to the first horizontal timing signal and the second horizontal timing signal such that each of the multiple horizontal clock signals has a different phase;

a means for selecting a multiple horizontal clock signal that is configured to select one of the multiple horizontal clock signals such that the occurrence of an edge corresponding to the selected horizontal clock signal is non-coincident with an edge associated with the vertical flyback signal; and

a means for producing a vertical blanking signal that is configured to produce a vertical blanking signal in response to the selected horizontal clock signal,

wherein the vertical blanking signal triggers the display device to count a predetermined number of blank horizontal lines from the top of the display screen prior to generating the OSD image such that the predetermined number of blank horizontal lines corresponds to the vertical position of the OSD image on the display screen, whereby jitter in the vertical position of the OSD window is reduced.

20. The apparatus of Claim 19, further comprising an interlace correction means that is configured to shift the phase of the multiple horizontal clock signals between each vertical frame period to compensate for a one-half line shift in the edge of the vertical flyback signal that occurs when the display device is in an interlace mode.

21. The apparatus of Claim 20, wherein the interlace correction means produces an interlace phase shift signal that is utilized by the clock signal generator to change the phase of each of the multiple horizontal clock signals.